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PTO/SB/05 (4/98)
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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 C.F.R. § 1.53(b))

Attorney Docket No.	LYTLE 18
First Inventor or Application Identifier	Steven A. Lytle
Title	DUAL DAMASCENE PROCESS WITH NO PASSING METAL FEATURES
Express Mail Label No.	EL344525265US

09/667046 09/21/00

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. [X] * Fee Transmittal Form *(e.g., PTO/SB/17)*
(Submit an original and a duplicate for fee processing)
2. [X] Specification [Total Pages 28]
(preferred arrangement set forth below)
- Descriptive title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings *(if filed)*
- Detailed Description
- Claim(s)
- Abstract of the Disclosure
3. [X] Drawing(s) *(35 U.S.C. 113)* [Total Sheets 4]
4. Oath or Declaration [Total Pages]
   a. [ ] Newly executed (original or copy)
   b. [ ] Copy from a prior application (37 C.F.R. § 1.63(d))
(for continuation/divisional with Box 16 completed)
      i. [ ] DELETION OF INVENTOR(S)
Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).

5. [ ] Microfiche Computer Program *(Appendix)*
6. Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)
   a. [ ] Computer Readable Copy
   b. [ ] Paper Copy (identical to computer copy)
   c. [ ] Statement verifying identity of above copies

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ACCOMPANYING APPLICATION PARTS

7. [ ] Assignment Papers (cover sheet & document(s))
8. [ ] 37 C.F.R.§3.73(b) Statement *(when there is an assignee)* [ ] Power of Attorney
9. [ ] English Translation Document *(if applicable)*
10. [X] Information Disclosure Statement (IDS)/PTO-1449 [X] Copies of IDS Citations
11. [ ] Preliminary Amendment
12. [X] Return Receipt Postcard (MPEP 503)
(Should be specifically itemized)
13. [ ] * Small Entity Statement(s) *(PTO/SB/09-12)* [ ] Statement filed in prior application, Status still proper and desired
14. [ ] Certified Copy of Priority Document(s)
(if foreign priority is claimed)
15. [ ] Other: .....

16. **If a CONTINUING APPLICATION,** *check appropriate box, and supply the requisite information below and in a preliminary amendment:*
[ ] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No: _____
Prior application information: *Examiner* _____ *Group / Art Unit:* _____

For CONTINUATION or DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 4b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

17. CORRESPONDENCE ADDRESS

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Signature	Charles W. Gaines	Date	09/21/2000

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FEE TRANSMITTAL for FY 2000

Patent fees are subject to annual revision.
Small Entity payments must be supported by a small entity statement, otherwise large entity fees must be paid. See Forms PTO/SB/09-12. See 37 C.F.R. §§ 1.27 and 1.28.

TOTAL AMOUNT OF PAYMENT ($) 834.00

Complete if Known	
Application Number	N/A
Filing Date	Herewith
First Named Inventor	Steven A. Lytle
Examiner Name	N/A
Group / Art Unit	N/A
Attorney Docket No.	LYTLE 18

METHOD OF PAYMENT (check one)

1. [X] The Commissioner is hereby authorized to charge indicated fees and credit any overpayments to:

Deposit Account Number: 12-2325

Deposit Account Name: Lucent Technologies

[X] Charge Any Additional Fee Required Under 37 CFR §§ 1.16 and 1.17

2. [ ] **Payment Enclosed:** [ ] Check [ ] Money Order [ ] Other

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	690	201	345	Utility filing fee	690.00
106	310	206	155	Design filing fee	
107	480	207	240	Plant filing fee	
108	690	208	345	Reissue filing fee	
114	150	214	75	Provisional filing fee	

SUBTOTAL (1) ($) 690.00

2. EXTRA CLAIM FEES

	Extra Claims		Fee from below	Fee Paid
Total Claims	28 -20** =	8	X 18.00	= 144.00
Independent Claims	3 - 3** =	0	X 78.00	= 0.00
Multiple Dependent				=

**or number previously paid, if greater; For Reissues, see below

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	78	202	39	Independent claims in excess of 3
104	260	204	130	Multiple dependent claim, if not paid
109	78	209	39	** Reissue independent claims over original patent
110	18	210	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 144.00

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet.	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	380	216	190	Extension for reply within second month	
117	870	217	435	Extension for reply within third month	
118	1,360	218	680	Extension for reply within fourth month	
128	1,850	228	925	Extension for reply within fifth month	
119	300	219	150	Notice of Appeal	
120	300	220	150	Filing a brief in support of an appeal	
121	260	221	130	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,210	241	605	Petition to revive - unintentional	
142	1,210	242	605	Utility issue fee (or reissue)	
143	430	243	215	Design issue fee	
144	580	244	290	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	690	246	345	Filing a submission after final rejection (37 CFR § 1.129(a))	
149	690	249	345	For each additional invention to be examined (37 CFR § 1.129(b))	

Other fee (specify) _____

Other fee (specify) _____

* Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 0.00

SUBMITTED BY

Complete *(if applicable)*

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Signature				Date	09/21/2000

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Attorney Docket No. LYTLE 18 PATENT APPLICATION

DUAL DAMASCENE PROCESS WITH NO PASSING METAL FEATURES

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CERTIFICATE OF EXPRESS MAIL

I hereby certify that this correspondence, including the attachments listed, is being deposited with the United States Postal Service, Express Mail - Post Office to Addressee, Receipt No. EL344525265US, in an envelope addressed to Commissioner of Patents and Trademarks, Washington, D.C. 20231, on the date shown below.

9-21-2000 Elizabeth Schumacher
Date of Mailing Typed or printed name of person mailing

Elizabeth Schumacher
Signature of person mailing

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DUAL DAMASCENE PROCESS WITH NO PASSING METAL FEATURES

TECHNICAL FIELD OF THE INVENTION

The present invention is directed, in general, to a semiconductor device and, more specifically, to an interconnect structure employing a dual damascene process with no passing metal features.

BACKGROUND OF THE INVENTION

Semiconductor devices, especially those that pertain to computer and telecommunications applications, have continued to be a focus for enhancing performance. Both smaller device size and higher speed of operation are performance targets. The success of many technology areas is dependent on the availability of high quality and cost effective integrated circuits. Transistors have been continually reduced in size as the ability to construct smaller gate structures has improved. As the size of transistors has decreased, the size of other components has become a limiting factor in increasing overall component densities.

Semiconductor devices employ a large number of openings in their design and manufacture. The size of these openings has been decreasing due to the demand for higher device packing densities

and therefore smaller device size. As the size of the openings decreases, the need increases for tighter control to assure proper device operation and therefore overall quality. Some of these openings are typically used to provide electrical contacts.

A key area controlling the overall quality and reliability of semiconductor devices is the area of interconnections between the various integrated components and circuits of the device. As is well known, vias are metal filled openings between the various layers of a semiconductor device that provide electrical connection between the layers at appropriate points. Trenches contain metal runners that are positioned in a layer to electrically interconnect appropriate points in the layer including vias. As the size of the openings decrease, accurate positioning of the holes for vias and the trenches for runners are more difficult to construct.

Current construction techniques for stacked vias typically use a small "landing pad" to assure that appropriate connections are aligned and made from layer to layer. The landing pads are larger than the diameter of the via holes to allow for some degree of misalignment and still accomplish a reliable electrical connection. Metal runners may be narrower in width than the landing pads. Thus, if the trench areas are exposed correctly in the photolithography process, the landing pad areas tend to be underexposed. In contrast, if the landing pad areas are exposed

correctly, the trench areas are usually overexposed. However, even if the landing pads and the trenches are the same width, the landing pads may be underexposed because generally they are much shorter. This disparate exposure effect creates the possibility of shorts across the landing pads and the runners.

To obviate the affects attributable to this disparate exposure effect, the industry has moved to biasing the reticle (photolithography mask), commonly using what is termed an optical proximity correction (OPC) technique. By biasing the landing pad features larger on the reticle, the exposure required for proper sizing of the trenches allows the landing pad areas to receive adequate exposure for the size needed, while at the same time adequately exposing the runner or trench areas. This solution, however, requires that spacing on the reticle be increased between openings and the runners or trenches, usually by a fixed margin or amount. As overall semiconductor device component size requirements continue to shrink, this fixed margin tends to become a limiting factor to minimizing component spacings.

Accordingly, what is needed in the art is a way to enhance the alignment process associated with the construction of vias and trenches without sacrificing critical space on the semiconductor wafer.

SUMMARY OF THE INVENTION

To address the above-discussed deficiencies of the prior art, the present invention provides a method of forming integrated circuit interconnect structures. In an exemplary embodiment, the method includes forming a via opening through first and second dielectric layers, such as silicon dioxide layers, located over a conductive layer, such as copper, and to a first etch stop layer, such as silicon nitride, located over the conductive layer. A trench opening is then formed through the second dielectric layer and to a second etch stop layer. In certain embodiments, the trench opening may be formed adjacent the via opening. Once the via and trench openings are formed, an etch is conducted that etches through the first etch stop layer such that the via opening contacts the underlying conductive layer.

Because the full via opening is etched before the formation of the trench, the photolithographic problems associated with the prior art methods are avoided. In fact, the design rules that require the trench to be a certain distance from the via can decreased because the over exposure or under exposure problems are substantially reduced, if not eliminated entirely.

In another embodiment, the via opening is a first via opening and forming the first via opening includes forming a second via

opening through the first and second dielectric layers and to the first etch stop layer. In another aspect of this particular embodiment, the trench is a first trench and forming a trench opening includes forming a second trench over the second via opening. The second via opening, in advantageous embodiments, will ultimately become an interconnect structure formed by a single or dual damascene process. The present invention is particularly advantageous when conducted with damascene processes. In yet another aspect of this particular embodiment, etching includes etching through the second etch stop in the first and second trench openings to the first dielectric layer.

In another advantageous embodiment, forming a trench includes depositing a photoresist over the second dielectric layer and in the via opening and forming an opening in the photoresist through which the trench opening is formed.

Another embodiment also includes forming the conductive layer, forming a first etch stop layer comprising silicon nitride over the copper, forming a first dielectric layer over the first etch stop layer, forming a second etch stop layer comprising silicon nitride over the first dielectric layer, and forming a second dielectric layer over the second etch stop layer, all prior to forming the via opening.

Once the various openings are formed, a conductive material, such as copper, may be deposited within the openings. Preferably, the conductive material is then planarized back to the second dielectric to form a substantially planar surface on which subsequent layers may be formed.

The foregoing has outlined, rather broadly, preferred and alternative features of the present invention so that those skilled in the art may better understand the detailed description of the invention that follows. Additional features of the invention will be described hereinafter that form the subject of the claims of the invention. Those skilled in the art should appreciate that they can readily use the disclosed conception and specific embodiment as a basis for designing or modifying other structures for carrying out the same purposes of the present invention. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the invention in its broadest form.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention is best understood from the following detailed description when read with the accompanying FIGUREs. It is emphasized that in accordance with the standard practice in the semiconductor industry the various features are not drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion. Reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

FIGURE 1 illustrates a partial sectional view of an exemplary embodiment of an interconnect structure formed in accordance with the principals of the present invention;

FIGURE 2 illustrates a partial sectional view of an interconnect structure formed at an intermediate stage of manufacture of the interconnect structure of FIGURE 1;

FIGURE 3 illustrates a partial sectional view of an interconnect structure showing formation of via openings in the interconnect structure of FIGURE 2;

FIGURE 4 illustrates a partial sectional view of an interconnect structure showing deposition and patterning of another photoresist layer to the interconnect structure of FIGURE 3;

FIGURE 5 illustrates a partial sectional view of an interconnect structure showing a dielectric etch that forms the trench openings to the interconnect structure of FIGURE 4;

FIGURE 6 illustrates a partial sectional view of an interconnect structure showing removal of the photoresist from the interconnect structure of FIGURE 5;

FIGURE 7 illustrate a partial sectional view of an interconnect structure showing an etch of the first and second etch stop layers for the interconnect structure of FIGURE 6; and

FIGURE 8 illustrates a partial sectional view of a combined interconnect structure incorporating an embodiment of the interconnect structure as shown in FIGURE 1, and a conventionally formed integrated circuit (IC) that may be used in conjunction with the present invention.

DETAILED DESCRIPTION

Referring initially to FIGURE 1, illustrated is a partial sectional view of an exemplary embodiment of an interconnect structure 100 formed in accordance with the principals of the present invention. The interconnect structure 100 includes a first metal feature 110 located on a surface of a semiconductor device, first and second etch stop layers 115, 125, first and second dielectric layers 120, 130. The interconnect structure 100 also includes a first via 140 that has a first portion that extends from the conductive layer 110 to the second etch stop layer 125 and a second portion that extends from the second etch stop layer 125 through the second dielectric layer 130. It should be noted that the via 140 does not have a landing pad, which may also be known as a passing metal feature, associated with it. In many conventional devices the landing pad is a metal-filled trench that is located immediately over a via and serves as a connection point for an overlying via. In such conventional devices, the trench portion is typically substantially wider than the lower via portion. The embodiment illustrated in FIGURE 1 further includes a first trench 150 approximate the first via 140 and a combined via/trench 145 having a second via 146 and a second trench 147. In an exemplary embodiment, the combined via/trench 145 may be a damascene

structure. In the illustrated embodiment, the interconnect structure 100 may be formed employing a method of the present invention further described in FIGUREs 2-7. The methods covered by the present invention that can be used to fabricate such a structure offer advantages over the prior art devices. For example, the first via 140 that passes through the first and second dielectric layer 120, 130 can be formed in a way to avoid the formation of a landing pad over the portion of the first via that extends under the second etch stop layer 125. Because the present invention provides a device that does not require a landing pad to join vias, the overexposure or underexposure problems associated with prior art methods can be avoided.

Turning now to FIGURE 2, illustrated is a partial sectional view of an interconnect structure 200 formed at an intermediate stage of manufacture of the interconnect structure 100 of FIGURE 1. The interconnect structure 200 includes the first metal feature 110, first and second etch stop layers 115, 125, first and second dielectric layers 120, 130 and a photoresist layer 210, all of which are deposited with conventional deposition processes and materials. The photoresist layer 210 is patterned for first and second via openings 215, 220 prior to the formation of any trenches.

In the illustrated embodiment, the first metal feature 110 is first formed by conventionally depositing a conductive layer of metal, such as copper. While the first metal feature 110 is shown as a continuous layer, it should be understood that this is for illustrative purposes only and that the first metal feature 110 will typically be patterned into multiple separate features. The first etch stop layer 115 is then conventionally formed over the conductive layer 110. Silicon nitride or other similar etch stop materials may be used. The first dielectric layer 120, which is typically silicon dioxide is then conventionally formed over the first etch stop layer 115. The second etch stop layer 125 is conventionally formed, also using silicon nitride, over the first dielectric layer 120. The second dielectric layer 130, which may also be comprised of silicon dioxide, is then formed over the second etch stop layer 125. Finally, the photoresist layer 210 is conventionally formed and patterned over the second dielectric layer 130 and patterned to locate the first and second via openings 215, 220.

The first and second dielectric layers 120, 130 may typically be formed through methods that include but are not limited to chemical vapor deposition, physical vapor deposition, such as high density plasma deposition processes, or a conventional spin on technique, to a thickness ranging from about 300 nm to about 1000

nm. The first and second etch stop layers 115, 125 may typically be deposited to a thickness ranging from about 15 nm to about 100 nm, by a conventional plasma enhanced chemical vapor deposition or other similar process.

The first metal feature 110, first and second etch stop layers 115, 125, and first and second dielectric layers 120, 130, are not limited to the materials disclosed above. For instance, the first metal feature 110 may include other appropriate conductor metals used in integrated circuit design as other applications or embodiments may require. Additionally, the first and second dielectric layers 120, 130 may also be formed from other appropriate dielectric materials. Alternatively, the first etch stop layer 115, located over the first metal feature 110, and the second etch stop layer 125 located over the first dielectric layer 120 may be formed from other available or future developed dielectric materials as well.

Turning now to FIGURE 3, illustrated is a partial sectional view of an interconnect structure 300 showing formation of via openings 315, 320 in the interconnect structure 200 of FIGURE 2. During this particular step, the via openings 315, 320 are formed down to the first etch stop layer 115. The first and second dielectric layers 120, 130 form an interface 305, which can include the second etch stop layer 125 in those embodiments where the

second etch stop layer 125 is present. However in other embodiments as illustrated below, the interface may simply be the plane at which the first and second dielectric layers 120, 130 contact each other. In the illustrated embodiment, it should be noted that the first and second via openings 315, 320 are formed through the first and second dielectric layers 120, 130, without first forming a landing pad at the interface 305. Thus, a landing pad located between the dielectric layers 120, 130 is not necessary. In other words, a landing pad formed in or on the upper surface of the first dielectric layer 120 is not necessary. The via openings 315, 320 are initially formed down to the first etch stop layer 115. The first and second dielectric layers 120, 130 are etched using a conventional dielectric etching process and the second etch stop layer 125 is also etched using conventional processes, such as by using a hexafluoride (SF_6) etch. Thus, if so desired, the first via 315 can be used as a pass through metal feature but because the via extends continuously through the first and second dielectric layer 120, 130, it is not necessary to form a landing pad trench between the portion of via 315 that extends under the second etch stop layer 125 and that portion of via 320 that extends above the second etch stop layer 125, as is conventionally done in prior art methods.

Turning now to FIGURE 4, illustrated is a partial sectional view of an interconnect structure 400 showing deposition and patterning of another photoresist layer to the interconnect structure 300 of FIGURE 3. A photoresist layer 410 is conventionally deposited and patterned for first and second trench openings 450, 445. In the illustrated embodiment, forming the first trench opening 450 includes first depositing the photoresist 410 over the second dielectric layer 130 and into the first via opening 315. Openings in the photoresist 410 are then formed for the first trench opening 450 and the second trench opening 445 over the second via opening 320. If the photoresist 410 is also initially deposited into the second via opening 320, it is typically removed when patterning the photoresist for the trench openings 445, 450, at this level. The second via opening 320, in advantageous embodiments, will ultimately become an interconnect structure formed by a dual damascene process. The present invention is, therefore, particularly advantageous when conducted with damascene processes, however, it is not limited to such applications. Typically at this point, conventional processes would pattern both the passing metal runner trench openings or landing pads at the same time using a biased reticle to achieve the desired degree of exposure for both the passing metal openings and

the trench. However, in the present invention, only the trench runner openings 450, 445, are patterned at this time.

Turning now to FIGURE 5, illustrated is a partial sectional view of an interconnect structure 500 showing a dielectric etch that forms trench openings 550, 547 to the interconnect structure 400 of FIGURE 4. The first trench opening 550 is formed adjacent the first via opening 315 through the second dielectric layer 130 and to the second etch stop layer 125. The second trench opening 547 is also formed through the second dielectric layer 130 and to the second etch stop layer 125. Again, since the first via opening 315 was formed prior to the first trench opening 550, the overexposure or underexposure issue associated with prior art processes are avoided, thereby maximizing the use of space on any given chip. Additionally, it should also be noted that the first via 315 is protected by the photoresist so that contact with conductive layer 110 is avoided while the trench 550 is etched.

Following the formation of the first trench opening 550 and the second trench 547, the photoresist 410 is conventionally removed and the openings 315, 550, 547 and 320 are cleaned, resulting in the structure shown in FIGURE 6.

Turning now to FIGURE 7, illustrated is a partial sectional view of an interconnect structure 700 showing an etch of the first and second etch stop layers for the interconnect structure 600 of

FIGURE 6 to form first and second via openings 740, 746 and first and second trench openings 750, 747. The first and second via openings 740, 746 are conventionally etched through the first etch stop layer 115 to the conductive layer 110 such that these openings contact the underlying conductive layer 110. Additionally, in an alternative embodiment, the first and second trench openings may be etched through the second etch stop layer 125 to the first dielectric layer 120. Once the various openings are formed, the conductive material, such as copper, may be deposited within the openings to form the interconnect structure 100 of FIGURE 1. Preferably, the conductive material is then planarized back to the second dielectric layer 130 to form the interconnect structure 100 as shown in FIGURE 1.

In summary, the embodiments of the present invention illustrated in FIGUREs 1-7 advantageously provide a situation where the full via opening is etched before the formation of the trench, thereby not requiring a landing pad trench to be formed, which in turn, avoids the photolithographic problems associated with the prior art methods. In fact, the design rules that require the trench to be a certain distance from the via can decrease, because the overexposure and underexposure problems may be substantially reduced, if not eliminated entirely.

FIGURE 8 illustrates a partial sectional view of a combined interconnect structure 800 incorporating an embodiment of the interconnect structure 100 as shown in FIGURE 1 and discussed above, and a conventionally formed integrated circuit (IC) 801 that may be used in conjunction with the present invention. While FIGURE 8 does not specifically illustrate how the interconnect structure described in FIGUREs 1-7 is electrically connected to the IC 801, one who is skilled in the art understands how to make such a connection, and integrate the interconnect structure, as provided herein, into the IC 801. The IC 801 includes conventional transistors 810 that are connected by a via 820, as covered by the present invention or by more conventional interconnects 825, such as damascene structures. The via 820 shows an illustrative embodiment of the present invention. As shown, the via 820 extends through dielectric layers 830 and 832 without a landing pad being present at the interface 833. Thus no landing pad is present in or on the upper surface of dielectric layer 830. However, a landing pad 836 may be located on or in the upper surface of dielectric layer 832 such that a via 838 formed within dielectric layer 834 may be more easily connected to the via 820. Dielectric layers 830, 832, 834 isolate the various layers of the IC 801. As illustrated, the transistors 810 are located on a semiconductor wafer substrate (generally designated 805), and the via 820, which

is located within the dielectric layers 830 832 connect the transistors 810 to different layers within the IC circuit 800.

Being of conventional design, forming the transistors 810 may include forming semiconductor devices, such as a complementary metal oxide semiconductor device, a merged bipolar and complementary metal oxide semiconductor device, or a bipolar semiconductor device. In the illustrated embodiment, the transistors 810 include conventionally formed tubs 835, source/drains 840, gate oxides 845 and gates 850. One who is skilled in the art knows how to fabricate the transistors 810 interconnects or vias 825 and dielectric layers 830, 832 and 834. Furthermore, it is also understood that multiple transistors 810, vias 820 and dielectric layers 830, 832, and 834, are typically interconnected to form the IC 801.

Although the present invention has been described in detail, those skilled in the art should understand that they can make various changes, substitutions and alterations herein without departing from the spirit and scope of the invention in its broadest form.

WHAT IS CLAIMED IS:

1. A method of forming an integrated circuit, comprising:

forming a via opening through first and second dielectric layers located over a conductive layer, the via extending through an interface of the first and second dielectric layers to form a passing metal feature of an interconnect structure; and

forming a trench in the second dielectric layer, wherein the trench opening is not formed at the interface of the first and second dielectric layers.

2. The method as recited in Claim 1 wherein the via opening is a first via opening and the method further includes forming a second via opening through the first and second dielectric layers.

3. The method as recited in Claim 2 wherein the trench is a first trench located approximate the first via opening and the method further includes forming a second trench over the second via opening.

4. The method recited in Claim 3 further including etching through an etch stop and to the first dielectric layer, the etch

stop located at the interface of the first and second dielectric layer.

5. The method as recited in Claim 1 wherein forming a trench includes depositing a photoresist over the second dielectric layer and in the via opening and forming an opening in the photoresist through which the trench is formed.

6. The method as recited in Claim 1 further including forming, prior to forming a via opening, the conductive layer, forming a first etch stop layer comprising silicon nitride over the conductive layer, forming a first dielectric layer over the first etch stop layer, forming a second etch stop layer comprising silicon nitride over the first dielectric layer, and forming a second dielectric layer over the second etch stop layer.

7. The method as recited in Claim 1 including forming a conductive copper layer and forming a first etch stop layer over the conductive copper layer and forming a second etch stop layer over the first dielectric layer.

8. The method as recited in Claim 1 further including depositing a conductive material in the via opening and the trench.

9. The method as recited in Claim 8 wherein depositing a conductive material includes depositing copper in the via opening and the trench.

10. The method as recited in Claim 1 wherein forming the via opening through the first and second dielectric layers includes forming the via with a single photolithographic mask.

11. A method of forming an integrated circuit, comprising:

forming a first dielectric layer over a first metal feature;

forming a second dielectric layer over the first dielectric layer; and

forming from a single photolithographic mask a via opening that extends through the first and second dielectric layers such that the via opening is void of a landing pad at an interface of the first and second dielectric layers, the via extending between the first metal feature and a second metal feature located over the second dielectric layer.

12. The method as recited in Claim 11 wherein the via opening is a first via opening and the method further includes forming a second via opening through the first and second dielectric layers and to a first etch stop layer located over the first metal feature.

13. The method as recited in Claim 12 further including forming a first trench approximate the first via opening and a second trench over the second via opening and to a second etch stop layer located over the first dielectric layer.

14. The method recited in Claim 11 further including forming a landing pad in a surface of the second dielectric layer, forming a third dielectric layer over the second dielectric layer and forming a via opening through the third dielectric layer and to the landing pad.

15. The method as recited in Claim 11 wherein forming a trench includes depositing a photoresist over the second dielectric layer and in the via opening and forming an opening in the photoresist through which the trench opening is formed.

16. The method as recited in Claim 11 further including forming, prior to forming a via opening, the first metal feature, forming a first etch stop layer comprising silicon nitride over the first metal feature, forming a first dielectric layer over the first etch stop layer, forming a second etch stop layer comprising silicon nitride over the first dielectric layer, and forming a second dielectric layer over the second etch stop layer.

17. The method as recited in Claim 11 wherein the first metal feature includes copper and the first and second dielectric layers includes silicon dioxide.

18. The method as recited in Claim 11 further including depositing a conductive material in the via opening.

19. The method as recited in Claim 18 wherein depositing a conductive material includes depositing copper in the via opening.

20. The method as recited in Claim 11 further including forming transistors selected from the group consisting of:

a complementary metal oxide semiconductor device,

a bipolar complementary metal oxide semiconductor device, and

a bipolar semiconductor device.

21. A semiconductor device, comprising:

a first metal feature located over a semiconductor surface and having a first dielectric layer located thereover and a second dielectric layer located over the first dielectric layer, the second dielectric layer having a second metal feature located in a surface thereof; and

a via located through the first and second dielectric layers, the via extending between and connecting the first metal feature and the second metal feature, the via being void of a landing pad between the first and second dielectric layers.

22. The semiconductor device as recited in Claim 21 wherein the via is a first via and the semiconductor device further includes a second via located through the first and second dielectric layers and wherein a trench structure is located over and connects with the second via.

23. The semiconductor device as recited in Claim 21 further including a trench structure located adjacent the via.

24. The semiconductor device as recited in Claim 21 wherein the via is a passing metal via with no passing metal feature.

25. The semiconductor device as recited in Claim 21 further including transistors wherein the first metal feature is located over the transistors and interconnects the transistors to form an operative integrated circuit.

26. The semiconductor device as recited in Claim 21 further including a damascene structure located adjacent the via.

27. The semiconductor device as recited in Claim 21 further including a third dielectric layer located over the second dielectric layer and a landing pad located between the second dielectric layer and the third dielectric layer.

28. The semiconductor device as recited in Claim 27 further including a via that extends through the third dielectric layer and contacts the landing pad.

DUAL DAMASCENE PROCESS WITH NO PASSING METAL FEATURES

ABSTRACT OF THE DISCLOSURE

The present invention provides a method of forming integrated circuit interconnect structures wherein a passing metal feature does not include a landing pad. In an exemplary embodiment, the method includes forming a via opening through first and second dielectric layers, such as silicon dioxide layer, located over a conductive layer, such as copper, and to a first etch stop layer, such as silicon nitride, located over the conductive layer. A trench opening is then formed through the second dielectric layer and to a second etch stop layer. Once the via and trench openings are formed, an etch is conducted that etches through the first etch stop layer such that the opening contacts the underlying conductive layer.

LTYLE 18

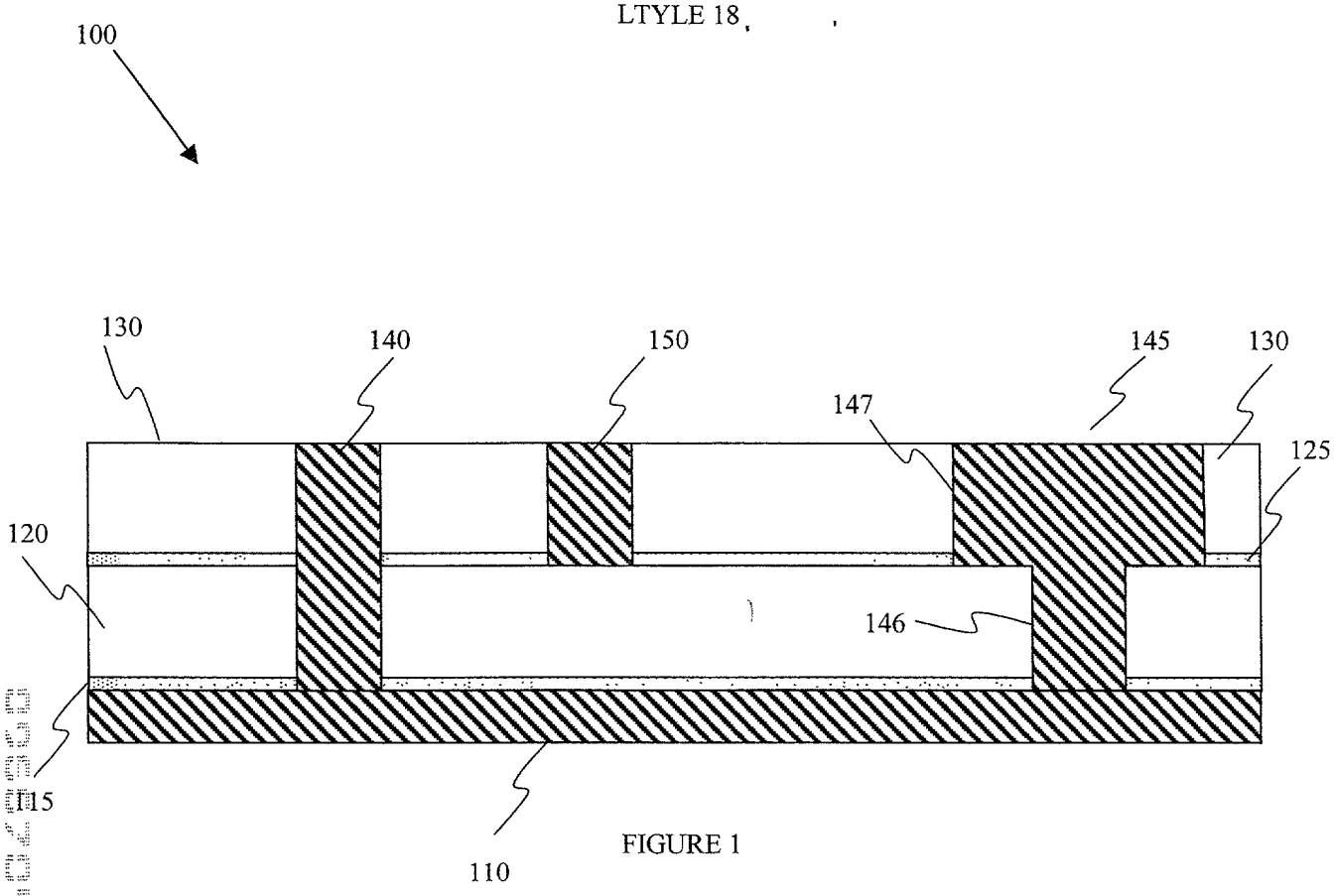

FIGURE 1

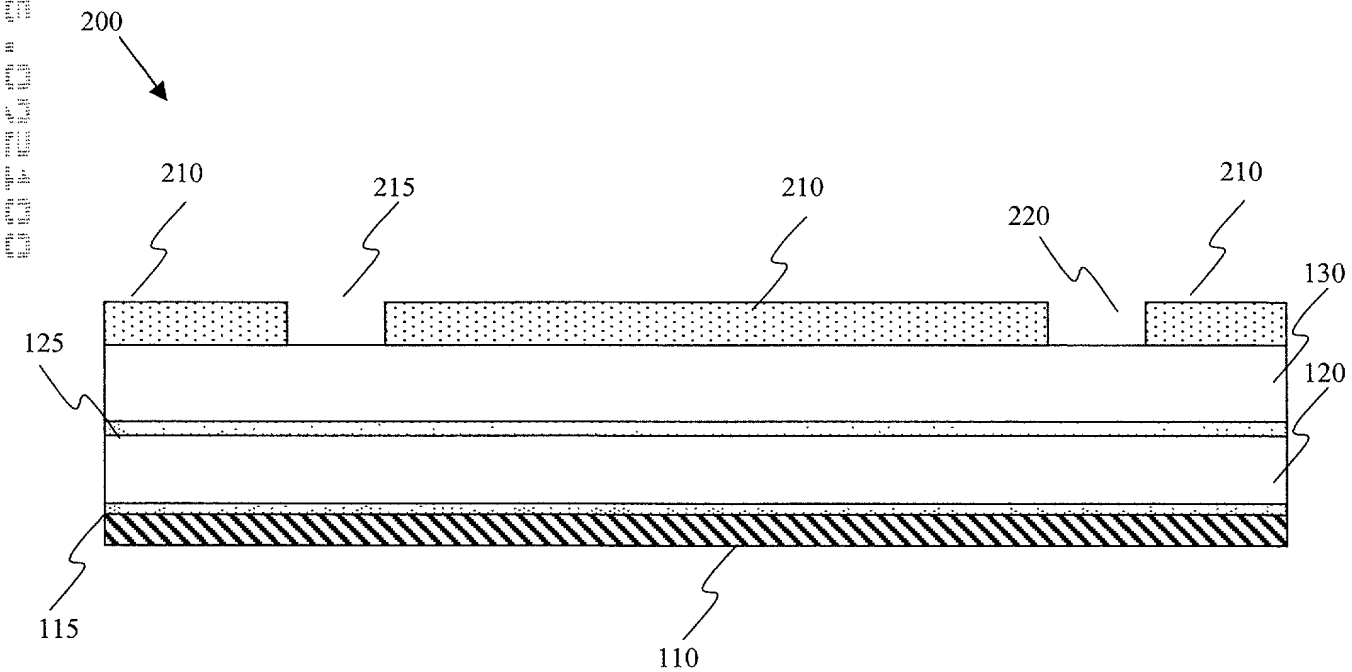

FIGURE 2

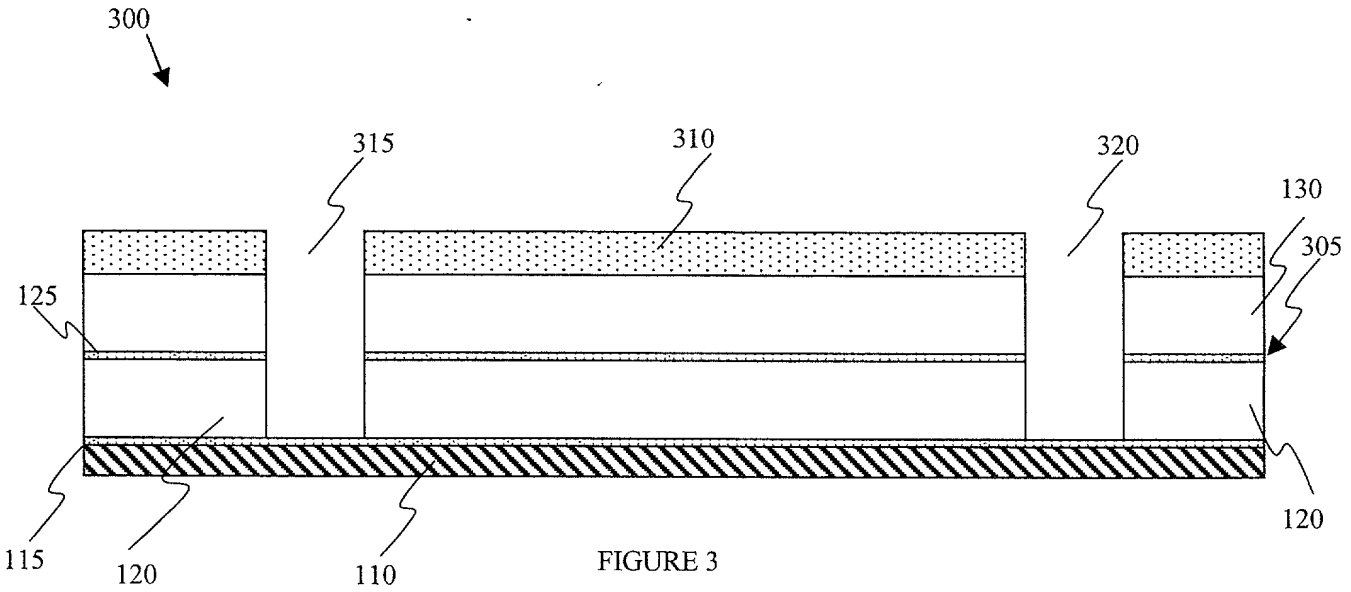

FIGURE 3

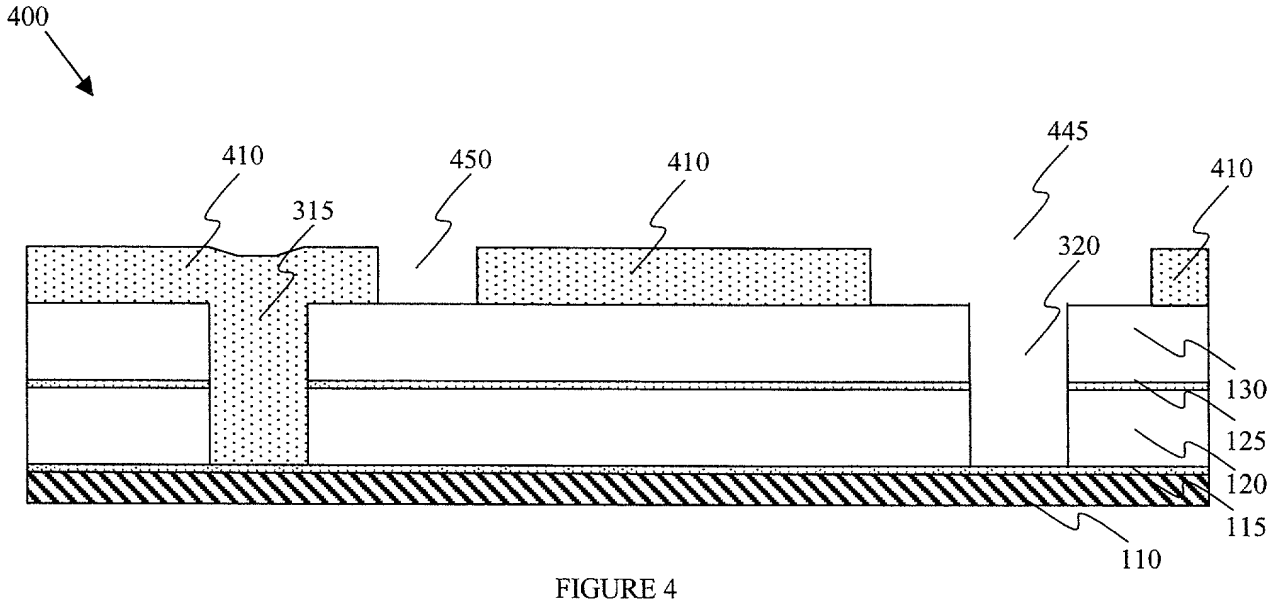

FIGURE 4

LTYLE 18.

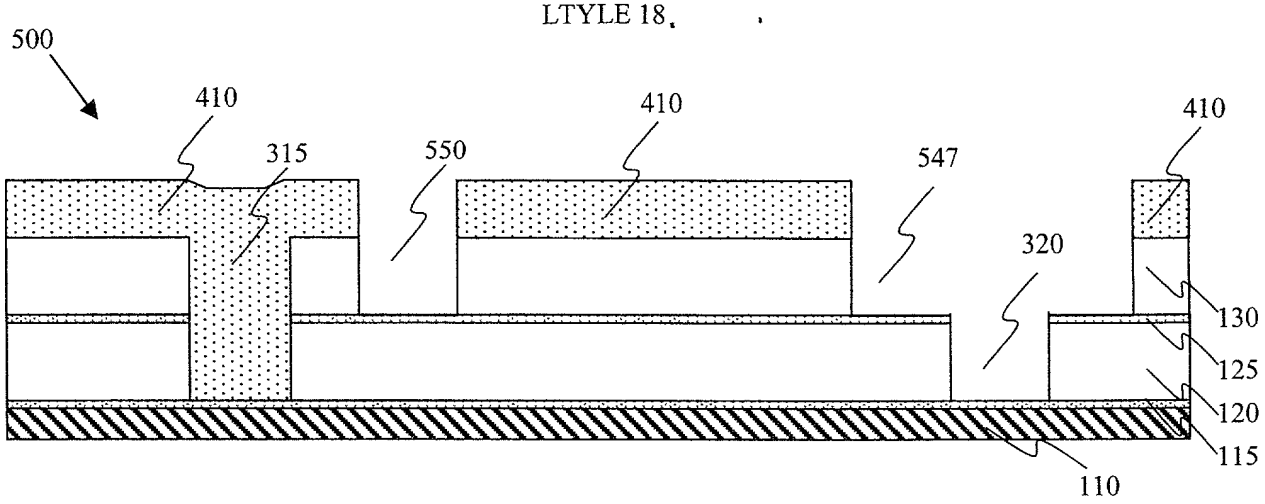

FIGURE 5

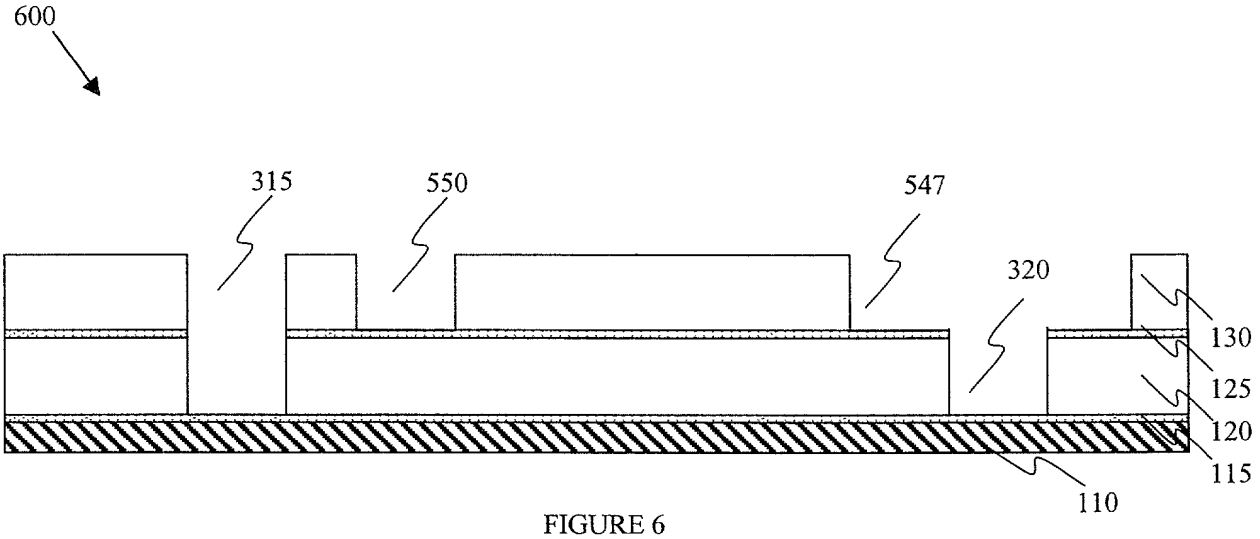

FIGURE 6

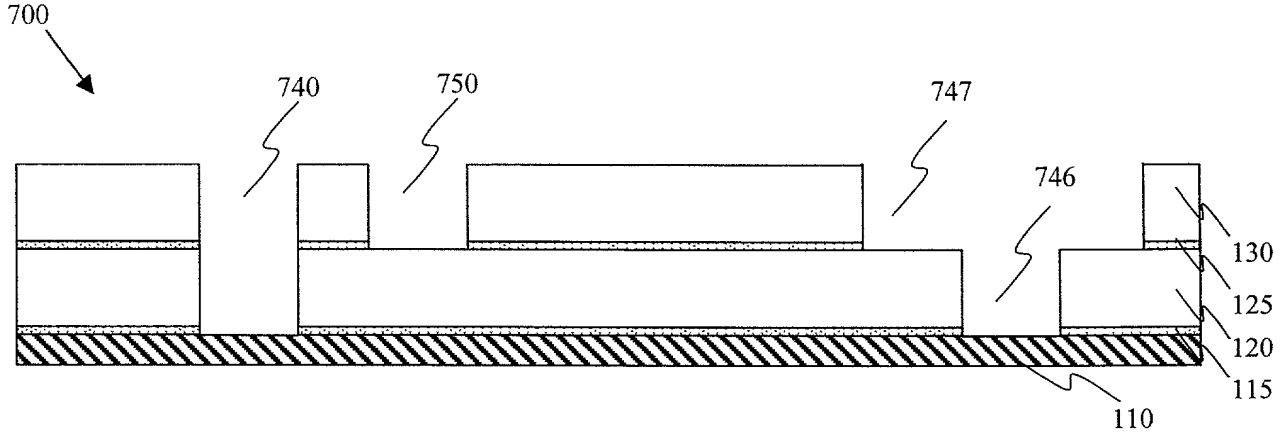

FIGURE 7

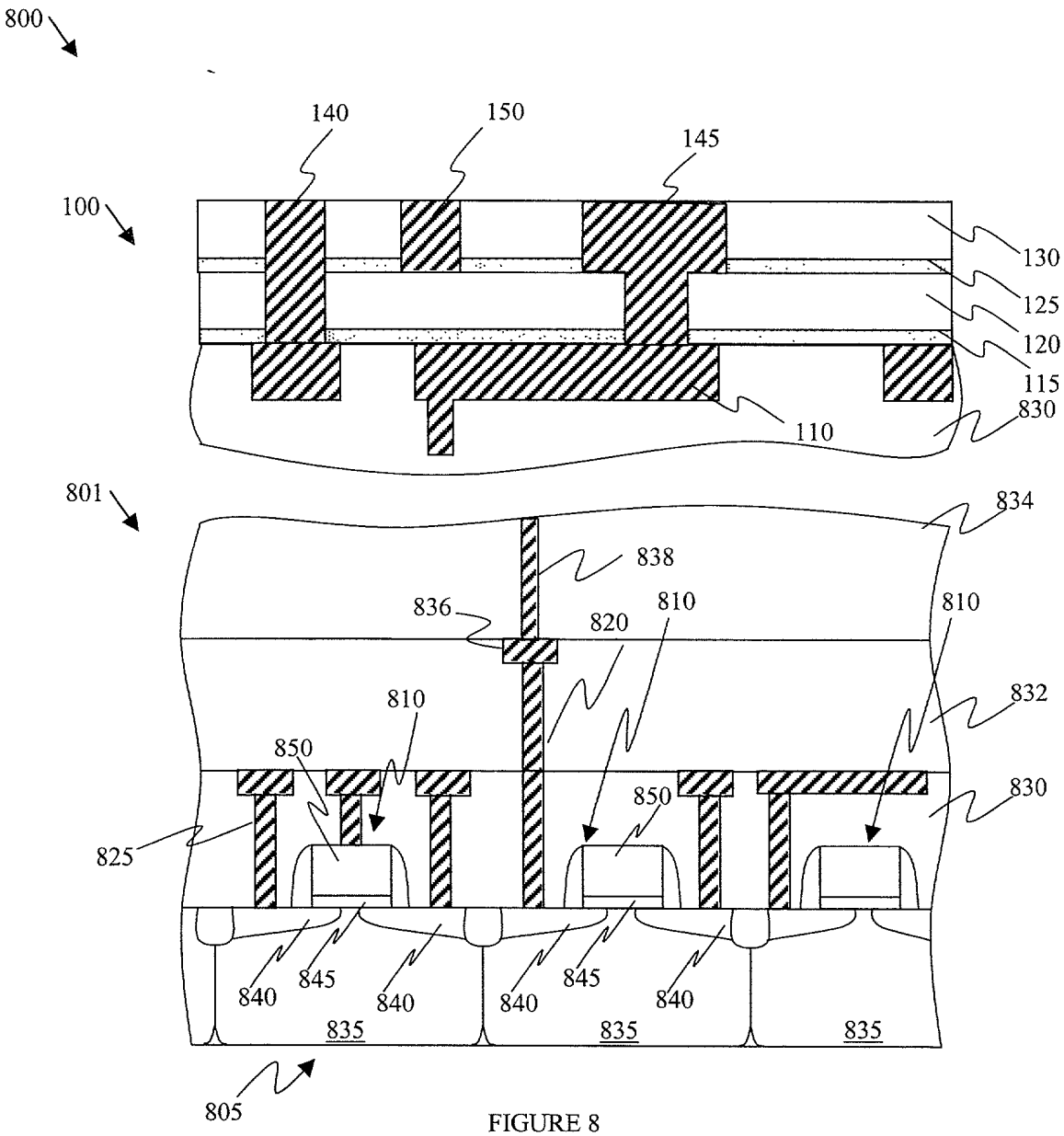
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FIGURE 8